

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory device comprising:
a plurality of memory cell arrays having a plurality of memory cells or memory cell units each of which include a plurality of memory cells, arranged in a matrix,
wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more different memory cell arrays, a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group, and the semiconductor memory device includes a memory chip including all of the plurality of memory cell array groups.

Claim 2 (Previously Presented): The semiconductor memory device according to claim 1, wherein the operation includes a parallel operation with respect to memory cells in two or more of the plurality of cell array groups.

Claim 3 (Previously Presented): The semiconductor memory device according to claim 1, wherein the operation includes a parallel operation with respect to memory cells in two or more of the plurality of cell arrays.

Claim 4 (Previously Presented): The semiconductor memory device according to claim 1, wherein the operation is a program or erase operation.

Claim 5 (Previously Presented): The semiconductor memory device according to claim 1, wherein the first Pass/Fail signal is a Pass/Fail signal indicating whether the

operation has attained success with respect to all of selected memory cells included in each of the cell array groups or not.

Claim 6 (Previously Presented): The semiconductor memory device according to claim 1, wherein a second Pass/Fail signal of an entire chip is also outputted when the first Pass/Fail signal is outputted.

Claim 7 (Previously Presented): The semiconductor memory device according to claim 1, wherein the first Pass/Fail signal is a Pass/Fail signal indicating whether the operation has attained success with respect to one memory cell array selected from the two or more memory cell arrays in each of the cell array groups or not.

Claim 8 (Previously Presented): The semiconductor memory device according to claim 1, wherein the first Pass/Fail signal is outputted after a first command is inputted.

Claim 9 (Previously Presented): The semiconductor memory device according to claim 8, wherein the first Pass/Fail signal is not outputted and a third Pass/Fail signal which is different from the first Pass/Fail signal is outputted after a second command is inputted.

Claim 10 (Previously Presented): The semiconductor memory device according to claim 8, wherein a forth Pass/Fail signal is outputted with respect to each of the cell arrays included in an entire chip after a third command is input.

Claim 11 (Previously Presented): The semiconductor memory device according to claim 10, wherein the third command is different from the first command.

Claim 12 (Previously Presented): The semiconductor memory device according to claim 1,

wherein the memory cell is EEPROM.

Claim 13 (Previously Presented): The semiconductor memory device according to claim 1, wherein the memory cell unit is a NAND cell type EEPROM.

Claim 14 (Cancelled).

Claim 15 (Currently Amended): A semiconductor memory device comprising:
a plurality of memory cell arrays having a plurality of memory cells or memory cell units each of which includes a plurality of memory cells, arranged in a matrix, wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more different memory cell arrays, the semiconductor memory device includes a memory chip including all of the plurality of memory cell array groups, and first Pass/Fail signals, each of which indicates success or failure of an operation of a respective one of the plurality of cell array groups, are output.

Claim 16 (Previously Presented): The semiconductor memory device according to claim 15, wherein the operation includes a parallel operation with respect to memory cells in two or more of the plurality of cell array groups.

Claim 17 (Previously Presented): The semiconductor memory device according to claim 15, wherein the operation includes a parallel operation with respect to memory cells in two or more of the plurality of cell arrays.

Claim 18 (Previously Presented): The semiconductor memory device according to claim 15, wherein the operation is a program or erase operation.

Claim 19 (Previously Presented): The semiconductor memory device according to claim 15, wherein the first Pass/Fail signal is a Pass/Fail signal indicating whether the operation has attained success with respect to all of selected memory cells included in each of the cell array groups or not.

Claim 20 (Previously Presented): The semiconductor memory device according to claim 15, wherein a second Pass/Fail signal of an entire chip is also outputted when the first Pass/Fail signal is outputted.

Claim 21 (Previously Presented): The semiconductor memory device according to claim 15, wherein the first Pass/Fail signal is a Pass/Fail signal indicating whether the operation has attained success with respect to one memory cell array selected from the two or more memory cell arrays in each of the cell array groups or not.

Claim 22 (Previously Presented): The semiconductor memory device according to claim 15, wherein the memory cell unit is a NAND cell type EEPROM.